**VERIFICATION OF KCL USING PSPICE**

**LAB # 06**



FALL 2023

**CSE103L Circuits & Systems-I Lab**

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Class Section: **B**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Submitted to:

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DATE: 20-MAY-2023

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**OBJECTIVES OF LAB**

* What is KCL?
* To verify KCL using pspice software.
* To know why KCL is also call as law of conservation of charge.

**KIRCHOFFS CURRENT LAW(KCL)**

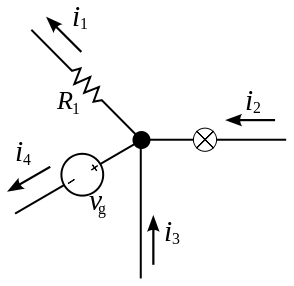
***Statement of* KCL**

This law states that in any electrical circuit at a node the algebraic sum of current entering the node is equal to algebraic sum of current leaving the node.

**MATHEMATICAL FORM**

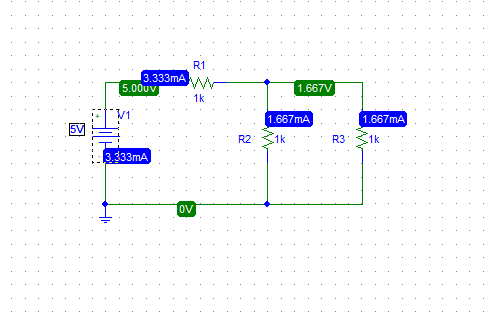
∑ Ientering=∑ Ileaving

CIRCUIT DAIGRAM:

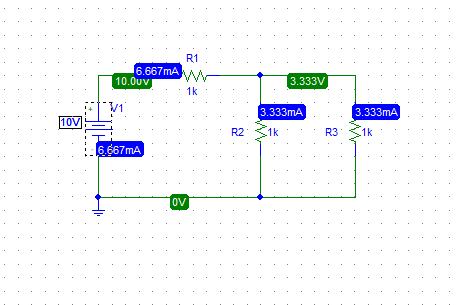


USING SAME RESISTANCE:

* 5V:



* 10V:



* 15V:

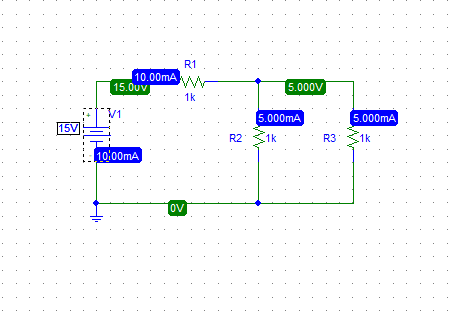
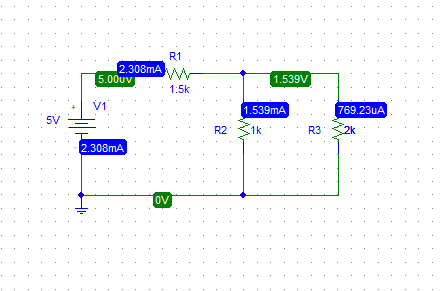


Table 1: Using Same Resistance:

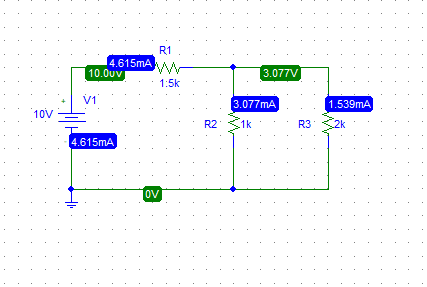
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S. No | V | R1 | R2 | R3 | I1 | I2 | I3 | I1=I2+I3 |
| 1 | 5 | 1k | 1k | 1k | 3.333A | 1.667A | 1.667A | 3.333=3.333 |
| 2 | 10 | 1k | 1k | 1k | 6.667A | 3.333A | 3.333A | 6.667=6.667 |
| 3 | 15 | 1k | 1k | 1k | 10A | 5A | 5A | 10=10 |

USING DIFFERENT RESISTANCE:

5V



* 10V



* 15V

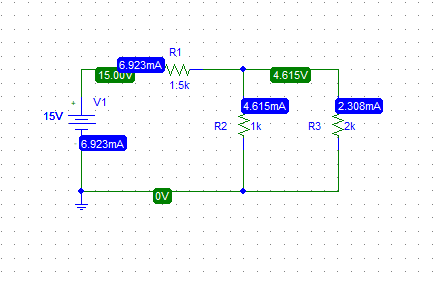


Table 2: Using Different Resistance:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S. No | V | R1 | R2 | R3 | I1 | I2 | I3 | I1=I2+I3 |
| 1 | 5 | 1.5k | 1k | 2k | 2.308mA | 1.539mA | 0.769A | 2.308=2.308 |
| 2 | 10 | 1.5k | 1k | 2k | 4.615mA | 3.3077mA | 1.539mA | 4.615=4.615 |
| 3 | 15 | 1.5k | 1k | 2k | 6.923mA | 4.615mA | 2.308mA | 6.923=6.923 |

ANALYSIS:

Kirchhoff's Current Law (KCL) states that the sum of currents entering a node or junction in a circuit must equal the sum of currents leaving that node or junction. Pspice is a popular computer-aided design (CAD) tool used for simulating and analyzing electronic circuits.

The goal of verifying KCL using Pspice is to ensure that the current values in a simulated circuit obey the law. This is typically done by creating a circuit in Pspice that contains several nodes, each with multiple branches. The current values in each branch are then calculated and compared to the current values in the neighboring branches to confirm that they add up to zero, indicating that KCL is being obeyed.

The verification process involves the following steps:

Creating the Circuit: The first step is to create a circuit in Pspice that contains multiple nodes and branches. The circuit can be designed using Pspice's schematic editor or by importing a netlist file that describes the circuit's topology.

Defining the Current Sources: Once the circuit is created, the current sources must be defined. These sources can be DC or AC sources and can be placed in any branch of the circuit.

Defining the Nodes: The next step is to define the nodes in the circuit. Each node is assigned a unique label, and the connections between nodes are defined using wires.

Running the Simulation: With the circuit set up and the current sources and nodes defined, the simulation can be run in Pspice. During the simulation, the current values in each branch of the circuit are calculated and displayed on the screen.

Analyzing the Results: Finally, the current values in each branch of the circuit are analyzed to ensure that they obey KCL. This is done by comparing the current values in each branch to the current values in the neighboring branches. If the sum of the current values entering a node equals the sum of the current values leaving that node, KCL is being obeyed.

In conclusion, verifying KCL using Pspice is a straightforward process that involves creating a circuit, defining the current sources and nodes, running the simulation, and analyzing the results. By verifying KCL, engineers can ensure that their circuits are functioning as expected and avoid potential problems caused by violating the law.

**LAB RUBRICS: (Circuits & Systems-I Lab)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Criteria & Point**  **Assigned** | **Outstanding**  **4** | **Acceptable**  **3** | **Considerable**  **2** | **Below Expectations**  **1** |
| **Attendance and Attentiveness in**  **Lab**  PLO10 | Attended in proper  Time and attentive in Lab | Attended in proper  Time but not attentive in Lab | Attended late but attentive in Lab | Attended late not attentive in Lab |
| **Equipment / Instruments Selection and Operation**  PLO1,  PLO2,  PLO3,  PLO5, | Right selection and operation of appropriate equipment and instruments to perform experiment. | Right selection of appropriate equipment and instruments to perform experiment but with minor issues in operation | Needs guidance for right selection of appropriate equipment and instruments to perform experiment and to overcome errors in operation | Cannot appropriately select and operate equipment and instruments to perform experiment. |
| **Result or Output/ Completion of target**  **in Lab**  PLO9, | 100% target has  been completed and well  formatted. | 75% target has been  completed and well formatted. | 50% target has  been completed but not well formatted. | None of the  outputs are  correct |
| **Overall, Knowledge**  PLO10, | Demonstrates excellent  knowledge of lab | Demonstrates good  knowledge of lab | Has partial idea about the Lab and  procedure followed | Has poor idea about the Lab and  procedure followed |
| **Attention to Lab Report**  PLO4, | Submission of Lab Report in Proper Time i.e. in next day of lab., with proper  documentation. | Submission of Lab Report in proper time but not with proper  documentation. | Late Submission  with proper  documentation. | Late Submission Very poor  documentation |